REMARKS

This is in response to the Office Action mailed April 18, 2007.

Claims 1 through 3 are currently pending in the application.

Claims 1 through 3 stand rejected. Applicant has amended claims 1, 2, and 3, and respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent 5,726,074 to Yabe in view of U.S. Patent 5,550,838 to Okajima

Claims 1 through 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yabe (U.S. Patent 5,726,074) in view of Okajima (U.S. Patent 5,550,838). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant further submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Turing to the cited prior art, the Yabe reference teaches or suggests the use of a bar code applied to a wafer to store information regarding the plurality of semiconductor integrated circuits formed on the wafer.

Applicant asserts that the Okajima reference teaches or suggests transferring data indicating a measurement status of a characteristics test of a semiconductor memory device is written into the semiconductor memory device.

Applicant asserts that the Yabe reference in view of the Okajima reference does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 2, and 3 because such cited prior art fails to teach or suggest

all the claim limitations of the claimed inventions. Applicant asserts that the Yabe reference does not teach or suggest the claim limitations of independent claims 1, 2, and 3 calling for "establishing an enhanced reliability testing flag for an integrated circuit device resulting from fabrication errors and manufacturing deviations from a manufacturing process for an integrated circuit device of a plurality of integrated circuit devices", "storing an enhanced reliability testing flag in the integrated circuit device associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires enhanced reliability testing" and "storing a reliability testing flag in the integrated circuit device associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires further reliability testing". In contrast to the claimed inventions of presently amended independent claims 1, 2, and 3 of the present application, neither the Yabe reference nor the Okajima reference nor any modification of the Yabe reference in view of the Okajima reference nor any combination of the Yabe reference and the Okajima reference teaches or suggests establishing an enhanced reliability testing flag for an integrated circuit device resulting from fabrication errors and manufacturing deviations from a manufacturing process for an integrated circuit device of a plurality of integrated circuit devices and stores such information on the semiconductor device. The Yabe reference uses a bar code regarding to store the speed of the semiconductor integrated circuit using bar code applied by a labeling machine 9B on the wafer, not the requirement of establishing an enhanced reliability testing flag for the semiconductor device for needing enhanced reliability testing and stored in the integrated circuit device associated with a unique identification code of each integrated circuit device. The Okajima reference merely stores test data in the semiconductor device. Applicant asserts that a bar code label installed on a wafer is not a code in an integrated circuit device as such in the claimed inventions of presently amended independent claims 1, 2, and 3 even if modified by the Okajima reference because there is no teaching or suggestion of an enhanced reliability testing flag. Therefore, such claims are allowable.

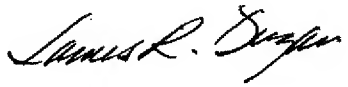
ENTRY OF AMENDMENTS

The amendments to claims 1, 2, and 3 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application to comply with the provisions of 35 U.S.C. § 132. Further, the amendments do not raise new issues or require a further search.

CONCLUSION

Claims 1 through 3 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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